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A method of forming a conductor wiring pattern,
                                                                                                                                                                                        forming a first insulating layer on a
                                          torming a rirst insulating a second,

torming a rirst insulating a second,

surface of a substrate and also forming a second,

surface of a substrate and rock, and recommendation and recommendation are recommendation.
                         comprising the following steps of:
                                                                                                                                                                                                                   light-exposing and developing the second
                                                     surrace or a supstrate and resin layer thereon;
photosensitive reacher and resin and r
                                                                          insulating layer to form pattern grooves so hat the
                                                                                    Insulating layer to form pattern grooves so that the exposed at bottoms of the first insulating
                                                                                                                                                                                                                                                             forming a plating seed layer on the second
                                                                                                                forming a plating seed layer on the pattern forming a plating inner surfaces of the plating inner surfaces on the plating layer including resist nattern on the plating layer forming a resist nattern and then forming a resist nattern on the plating layer and then forming a resist nattern on the plating layer including the forming a resist nattern on the plating layer including the forming a resist nattern on the pattern on the plating layer including the pattern on the pattern on the pattern on the plating layer on the pattern on the plating including inner surfaces of the plating inner surfaces of t
                                                                                                                           insulating layer including a resist pattern arrower.

Insulating then for nortions of the nattern arrower.

grooves and then for nortions of the nattern arrower.
                                                                                                                                     grooves and then for portions of the pattern arrows with a seed layer except filling the pattern arrows with a
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                                                                                                                                                        conductor by an electrolytic plating and sever a nower events.
                                                                                                Pattern grooves;
                                                                                                                                                                                      removing the seed layer to form "iring nathorn consisting 
                                                                                                                                                                                                removing the seed layer to form wiring arrower second insulating remained in the nattern arrower of conductors remained in the nattern arrower.
                                                                                                                                                                     seed layer as a power supply layer;
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                                                                                                                                                                                                           second insulating layer to form wiring partern grooves.

of conductors remained in the pattern grooves.
                                                                                                                                                                                                                                                                                                                     tour remarked the forth in claim 1, wherein a set forth in claim 1, wherein a A method as set
                                                                                                                                                                                                                            2. A method as set forth in claim 1, where in a the forth in claim 1, where in the ase used, as the filled with the plurality of different method arounder are filled with the plurality when the nattern arounder are filled with the plurality when the nattern arounder are filled with the plurality when the nattern arounder are filled with the plurality when the nattern arounder are filled with the plurality when the nattern arounder are filled with the plurality when the nattern arounder are filled with the plurality where it is not all the plurality when the plurality where it i
                                                                                                                                                                                                                                       Plurality of different metal layers are filled with the conductor, when the electrolytic plating.
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                                                                                                                                                                                                                                                                                                                                                          by the electrolythic plating. Wherein the A method as set and a set and a set and a set and a set a se
                                                                                                                                                                                                                                                                    A method as set torth in claim at least two are not and a different metal layers are a lawer and a plurality of different metal are a conser have lawer and a plurality of a conservation of a c
                                                                                                                                                                                                                                                  conductor by the electrolytic plating.
                                                                                                                                                                                                                                                                             plurality or consisting of a copper base layer and a metal layers haver
                                                                                                                                                                                                                                                                                                                                                                                                rrier layer. set forth in claim 1, wherein the
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                                                                                                                                                                                                                                                                                                             A method as set forth in claim 1, wherein the a method as set forth in claim 1, wherein the first insulating layer is composed of a photosensitive first insulating regin:
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     after the first insulating layer is light after
                                                                                                                                                                                                                                                                                                                                          exposed and developed to formed on the substrate is to be
                                                                                                                                                                                                                                                                                             nickel barrier layer.
                                                                                                                                                                                                                                                                                                                                                     exposed and developed to form an opening, through which to be first wiring pattern to a second wiring 
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                                                                                                                                                                                                                                                                                                                                                              first wiring pattern formed on the substrate 1s to be second wiring pattern to be second wiring pattern the first law connected to a second laver the first electrically connected inculation laver the first electrically first inculation
                                                                                                                                                                                                                                                                                                                                                                        electrically connected to a second wifiling patceri the first insulating layer, the first formed on the first insulating layer,
                                                                                                                                                                                                                                                                                                                             insulating resin:
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insulating layer is heated and hardened.

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5. A method as set forth in claim 1, wherein a semiconductor wafer is used as the substrate, the semiconductor wafer has an electrode terminal forming surface, on which the first insulating layer and the second insulating layer are formed, and the wiring pattern, which is electrically connected with electrode terminals of the semiconductor wafer, is formed.